



Heller Ehrman White & McAuliffe LLP
Title: "REFERENCE WAFER AND PROCESS FOR
MANUFACTURING SAME"
Inventor(s): A. Smith et al.
Atty Docket No.: 38203-6081B
Application No.: 10/765,223 - Filed: 01/26/2004
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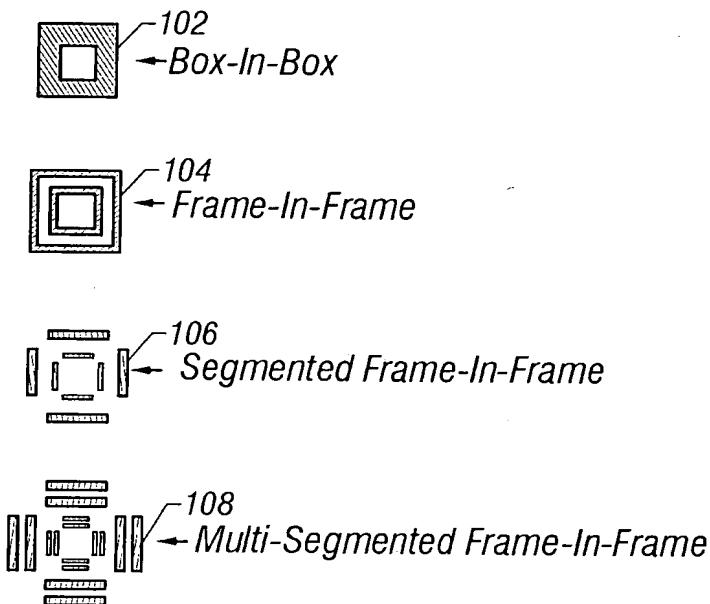


FIG. 1

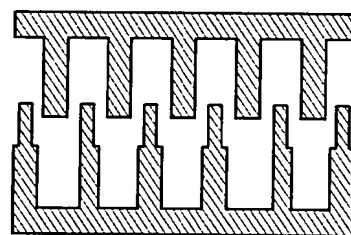


FIG. 2

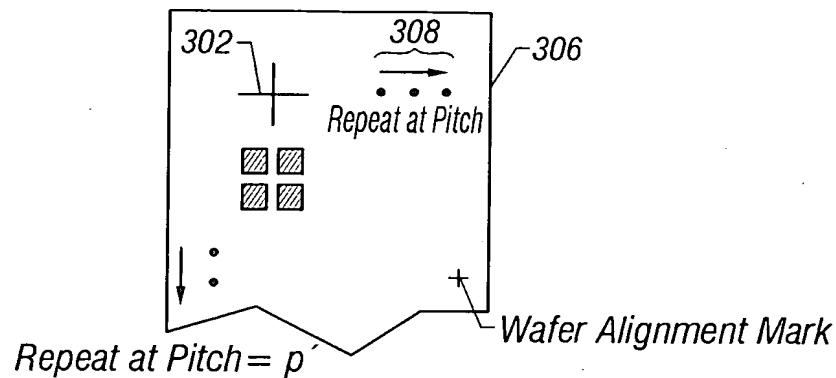


FIG. 3

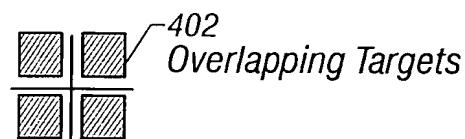


FIG. 4

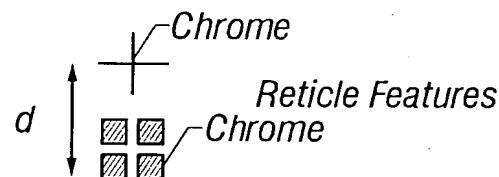


FIG. 5A

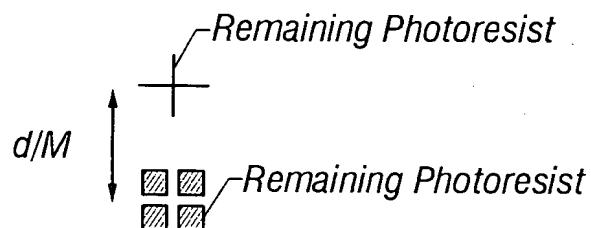


FIG. 5B

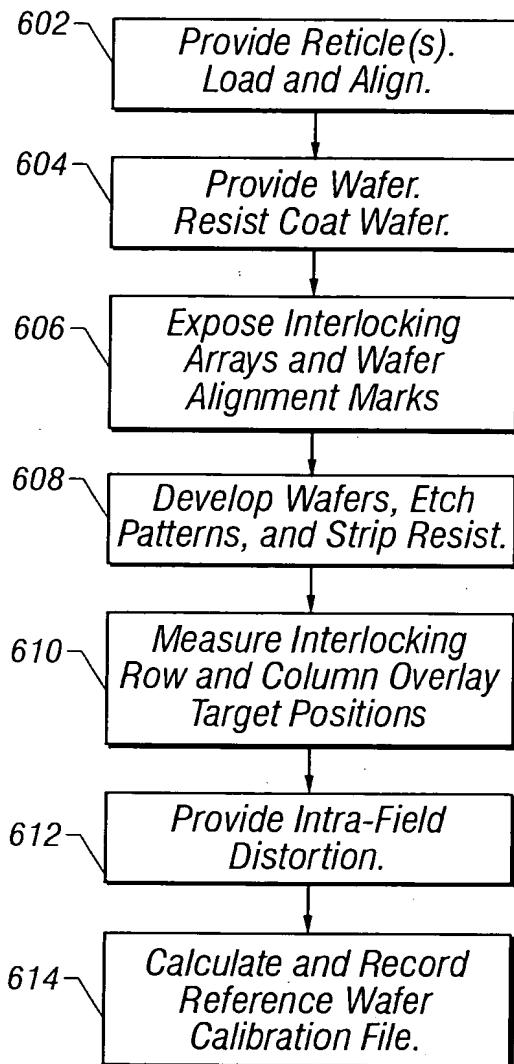


FIG. 6

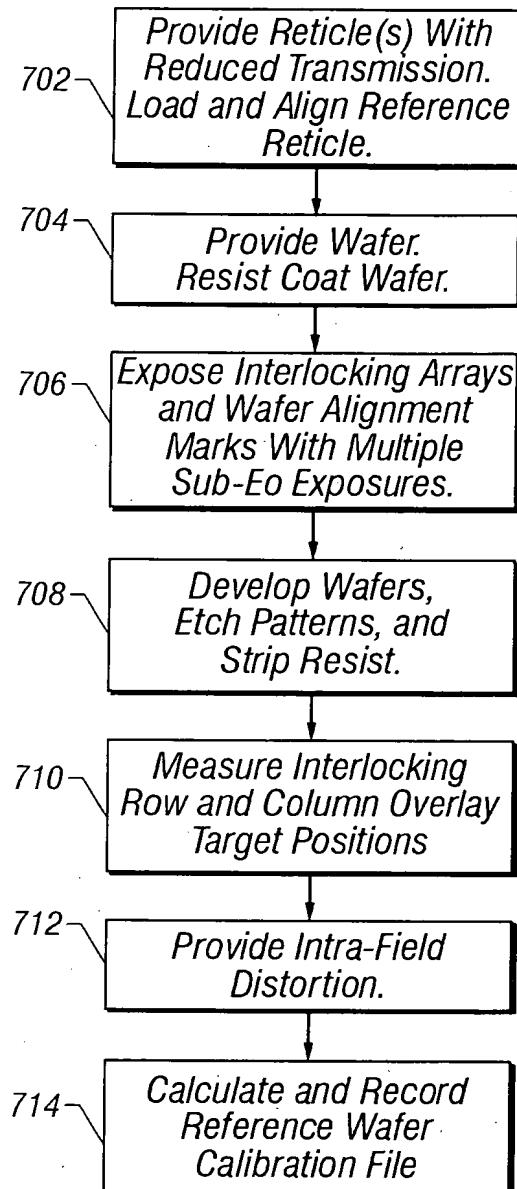


FIG. 7

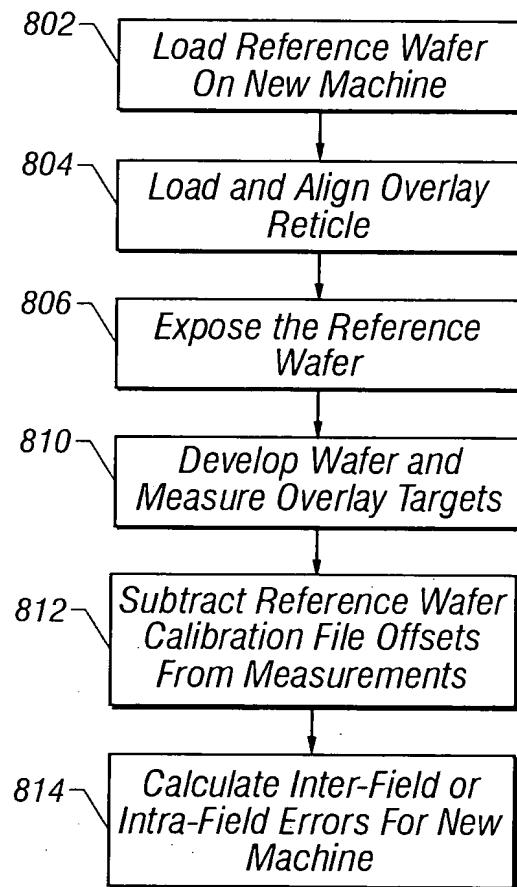


FIG. 8

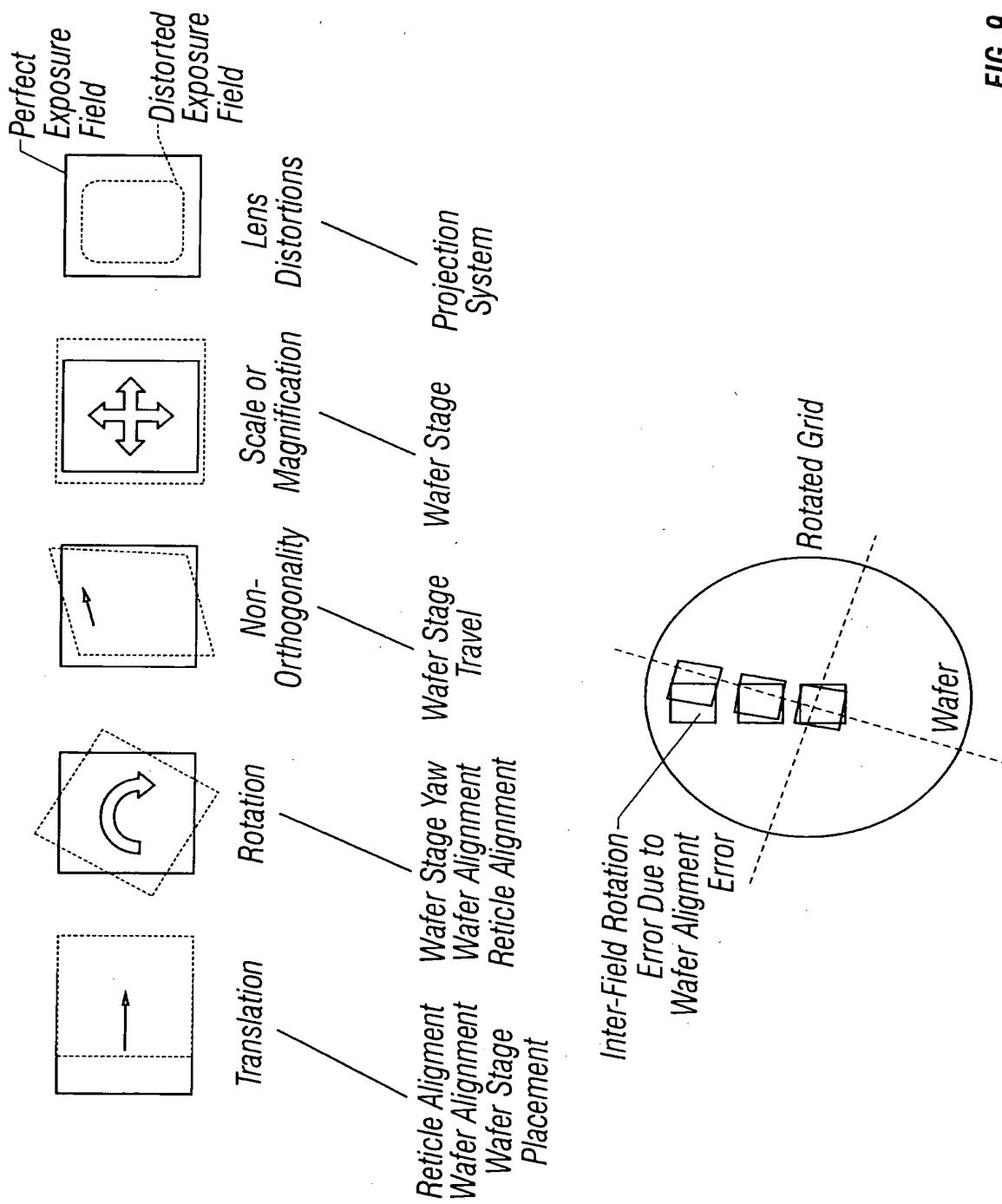


FIG. 9

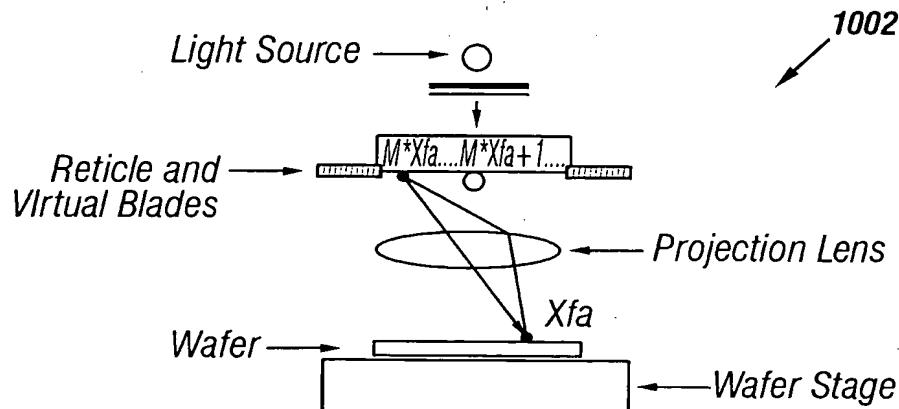


FIG. 10

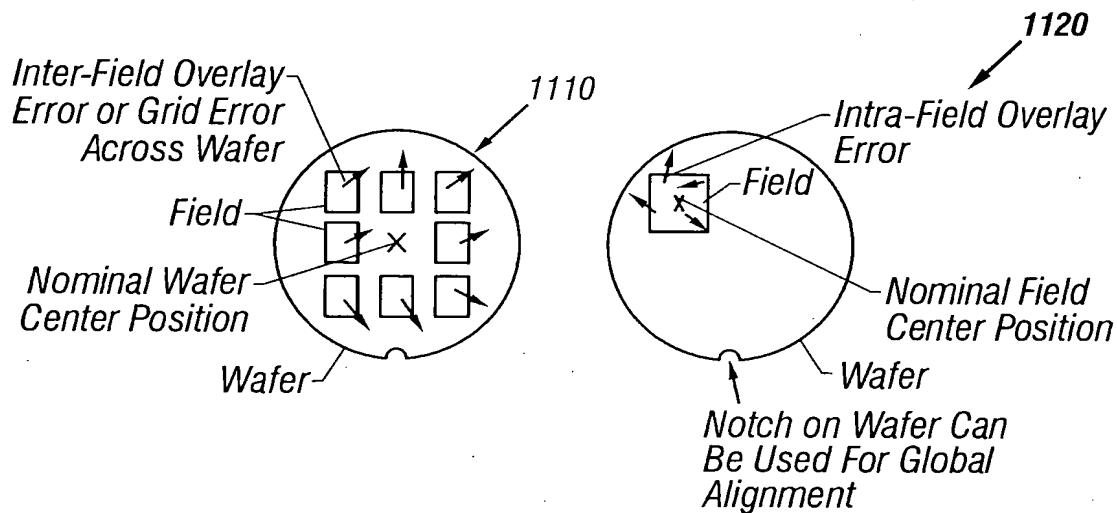


FIG. 11A

Zero Yaw=Solid Line Fields
 Non-Zero Yaw=Dashed Fields

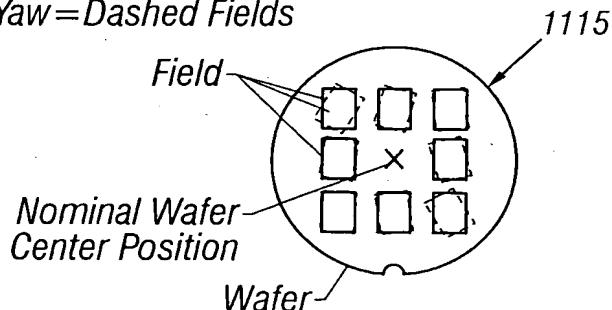


FIG. 11B

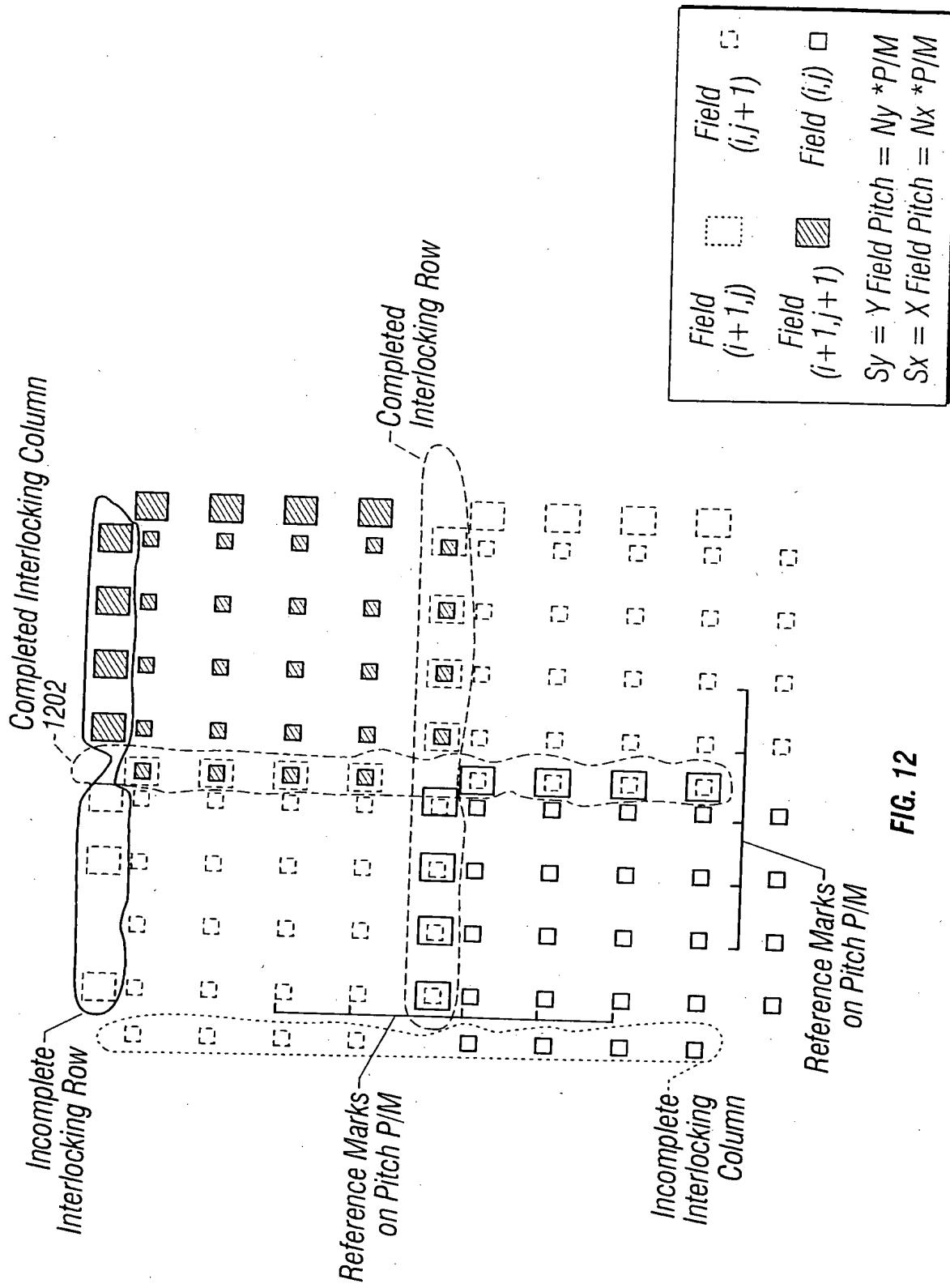


FIG. 12

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FIG. 13A Reference Mark, One of $N_x \times N_y$ Interlocking Array Reticule 1310

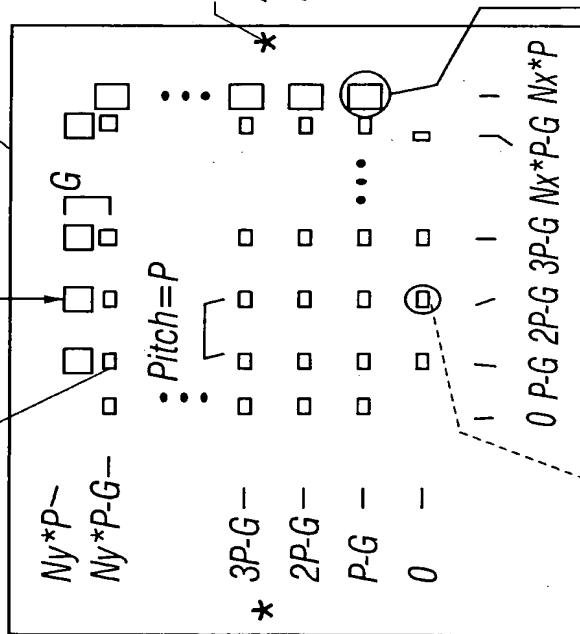
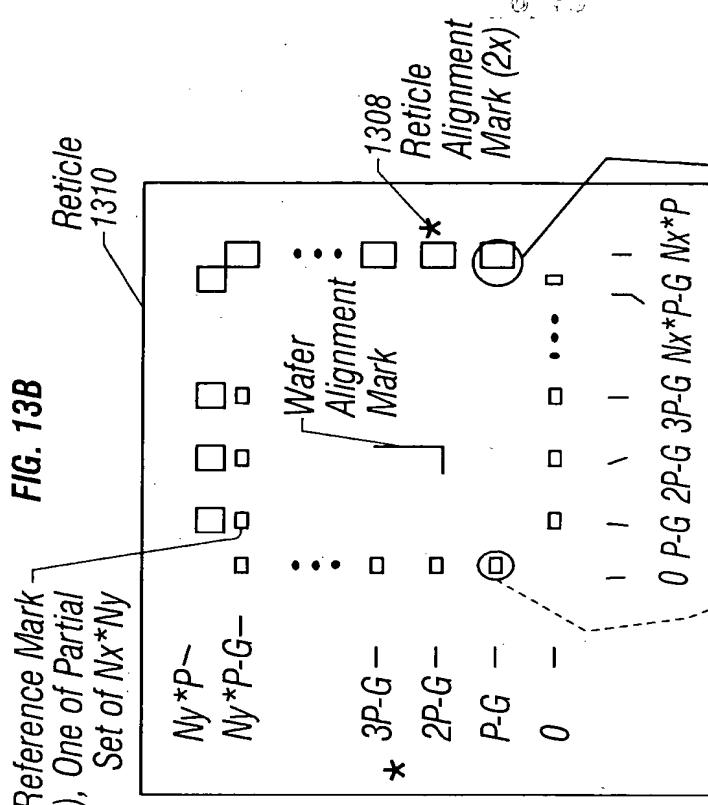


FIG. 13B



Inner Box. 40um x 40um
 Outer Box 96um x 96 um
1306 

FIG. 13C

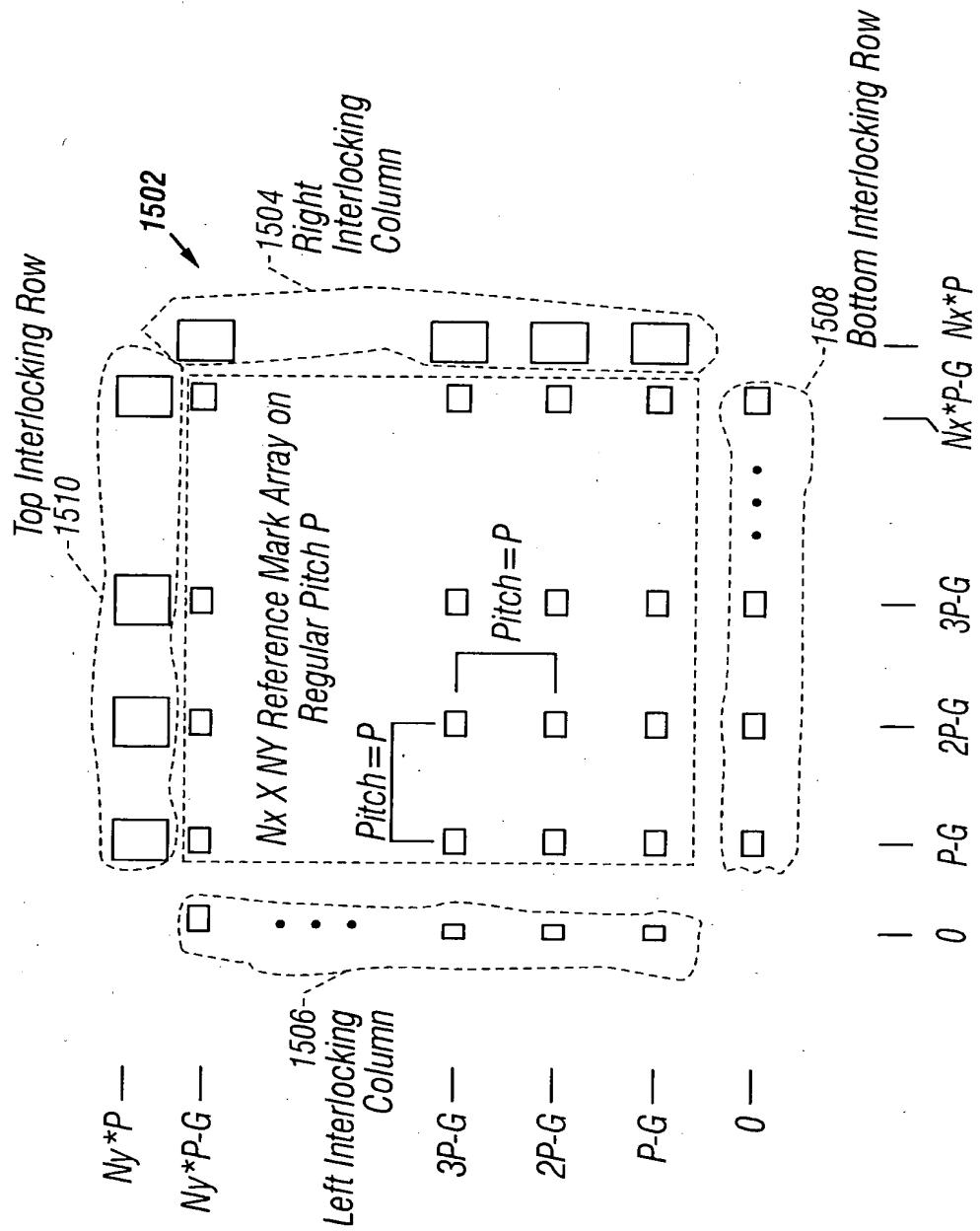


FIG. 15

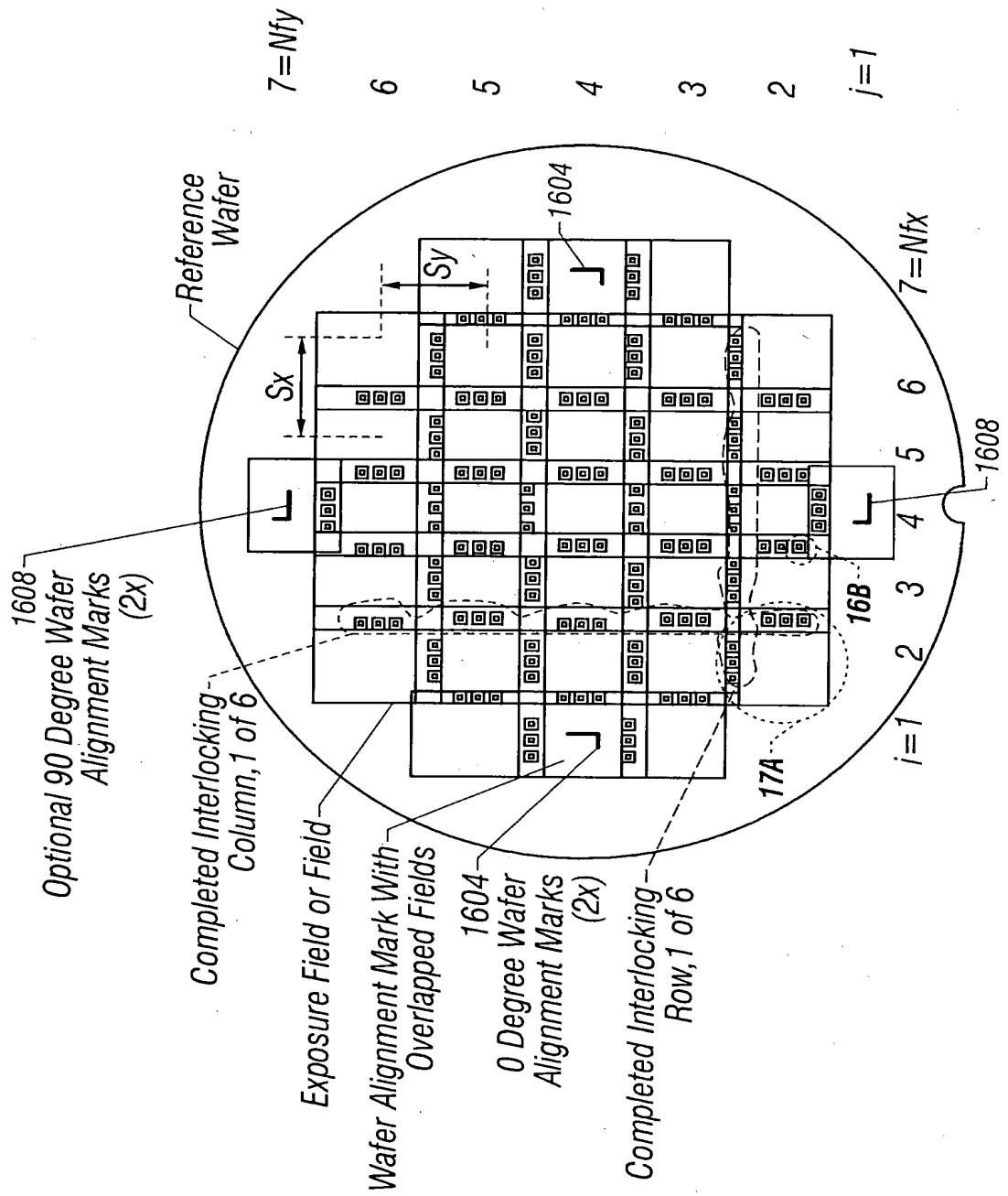


FIG. 16A

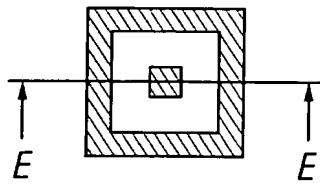


FIG. 16B



FIG. 16C

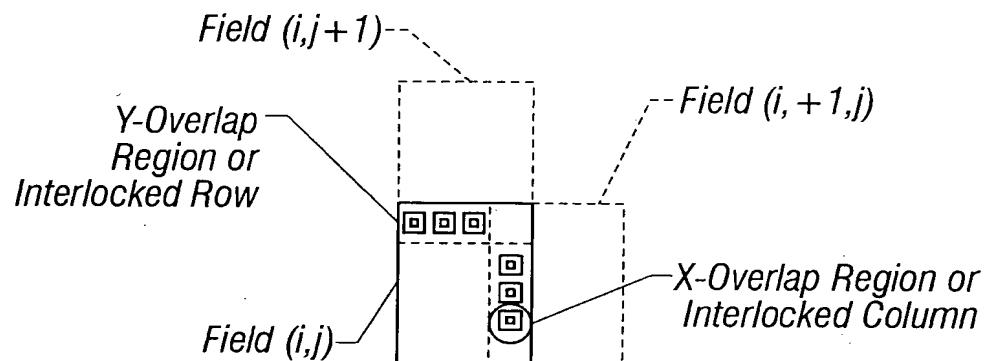


FIG. 17A

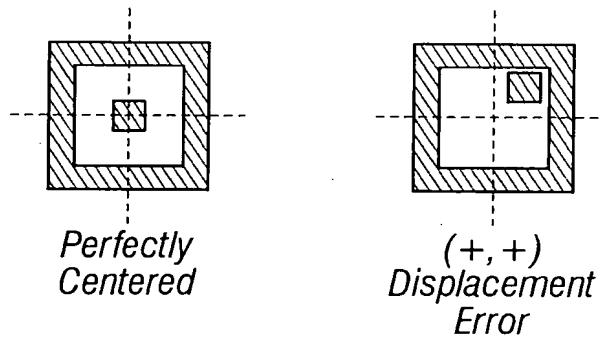


FIG. 17B

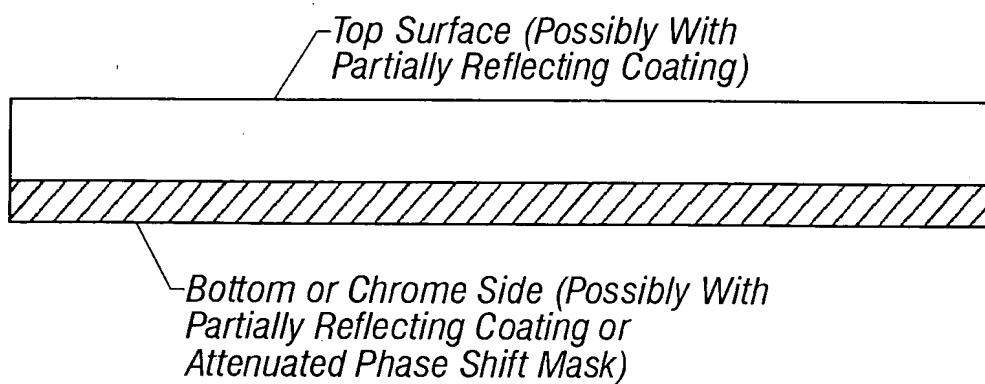


FIG. 14

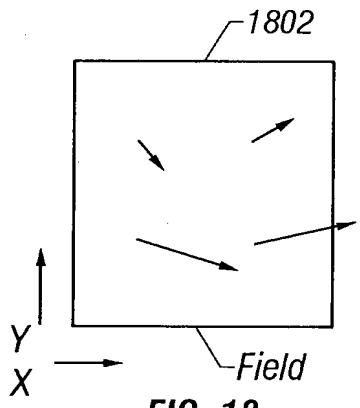


FIG. 18

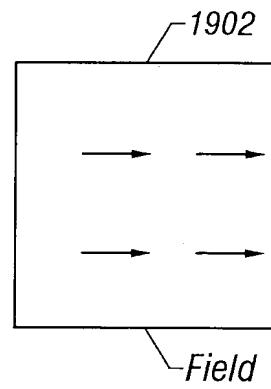


FIG. 19

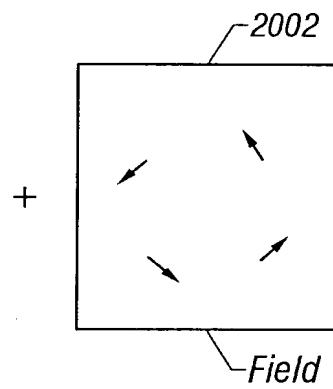


FIG. 20

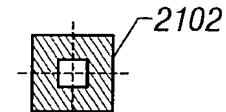
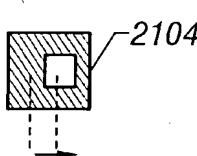


FIG. 21

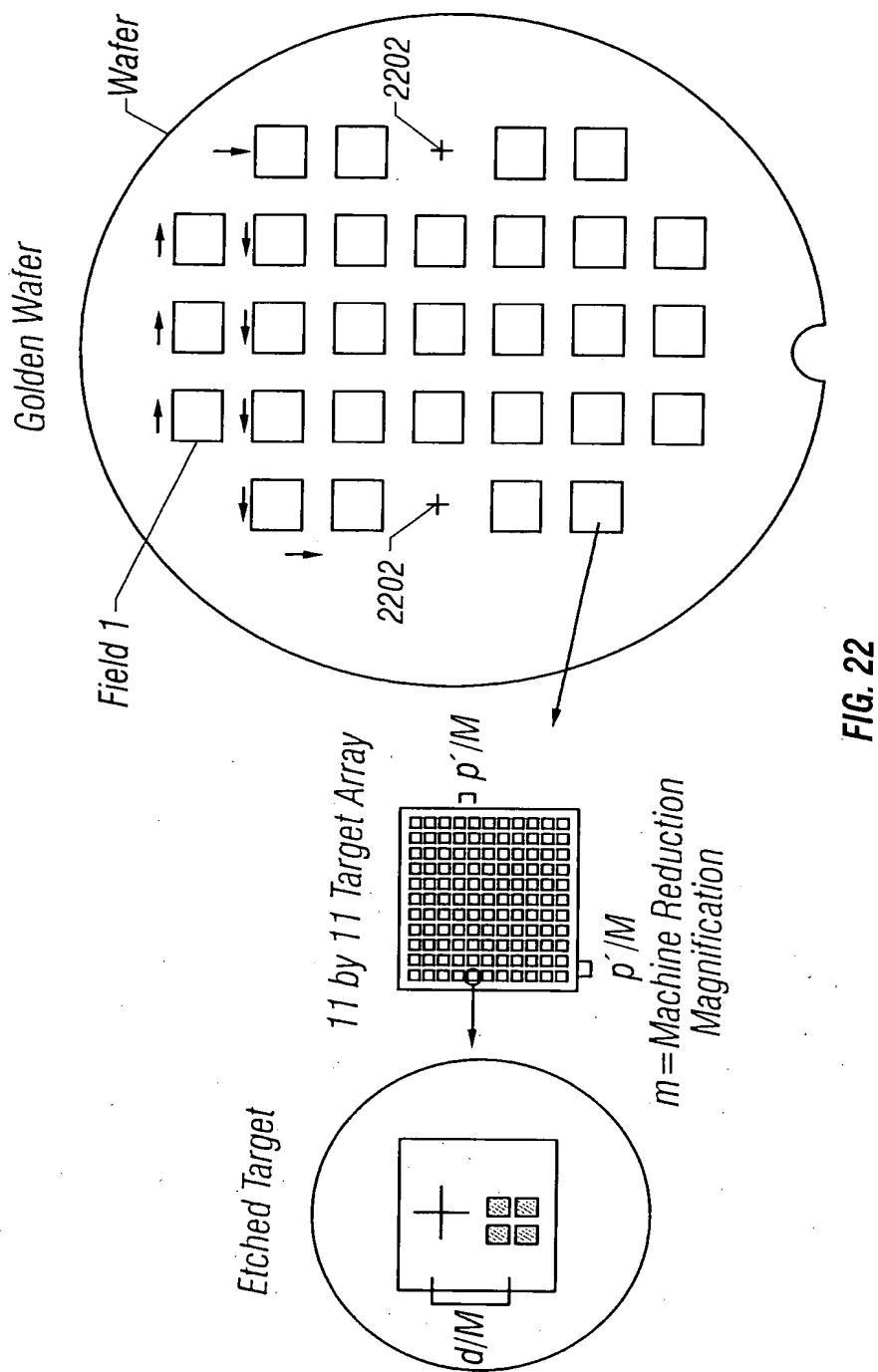


FIG. 22

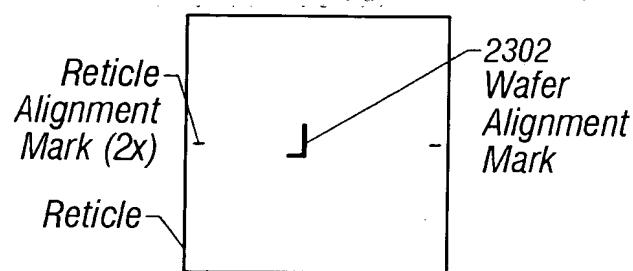


FIG. 23

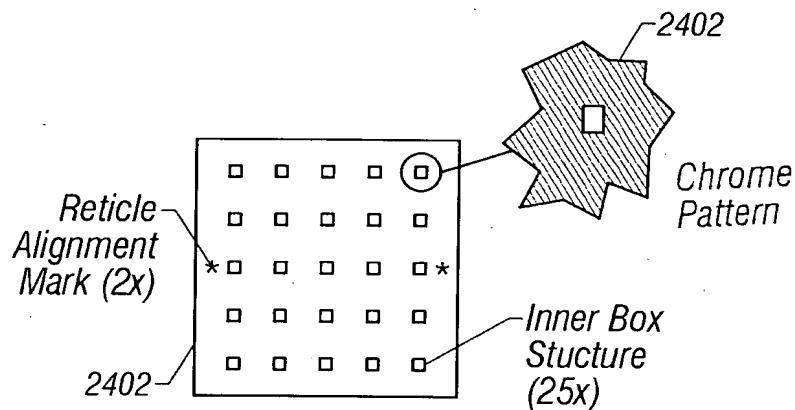


FIG. 24

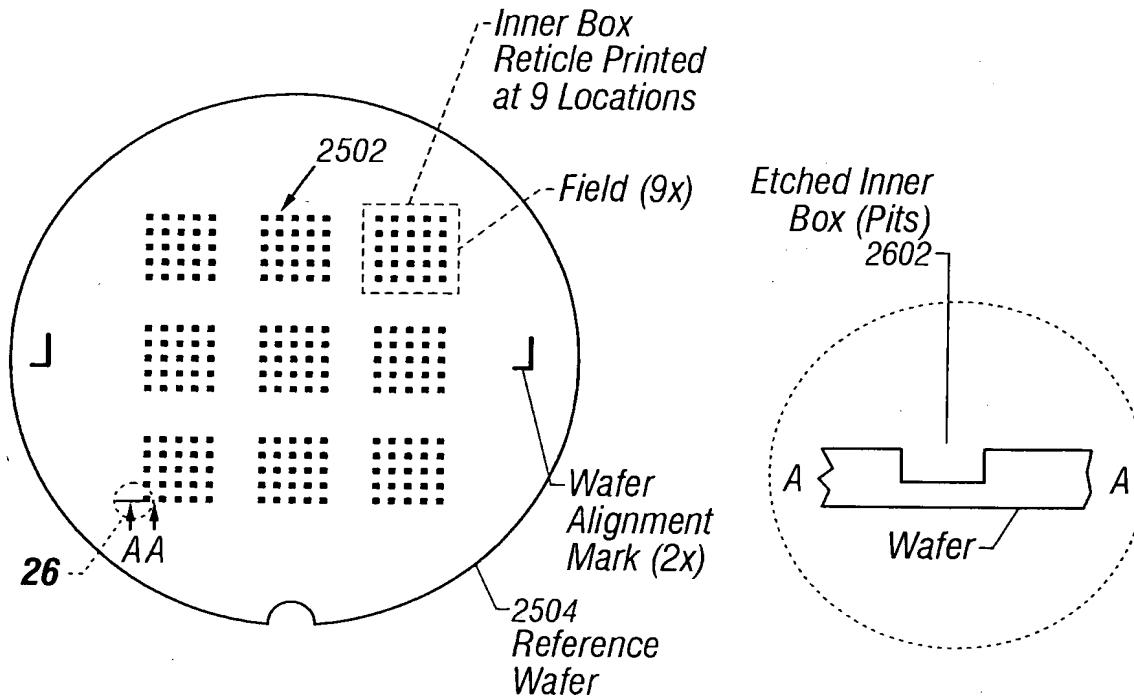
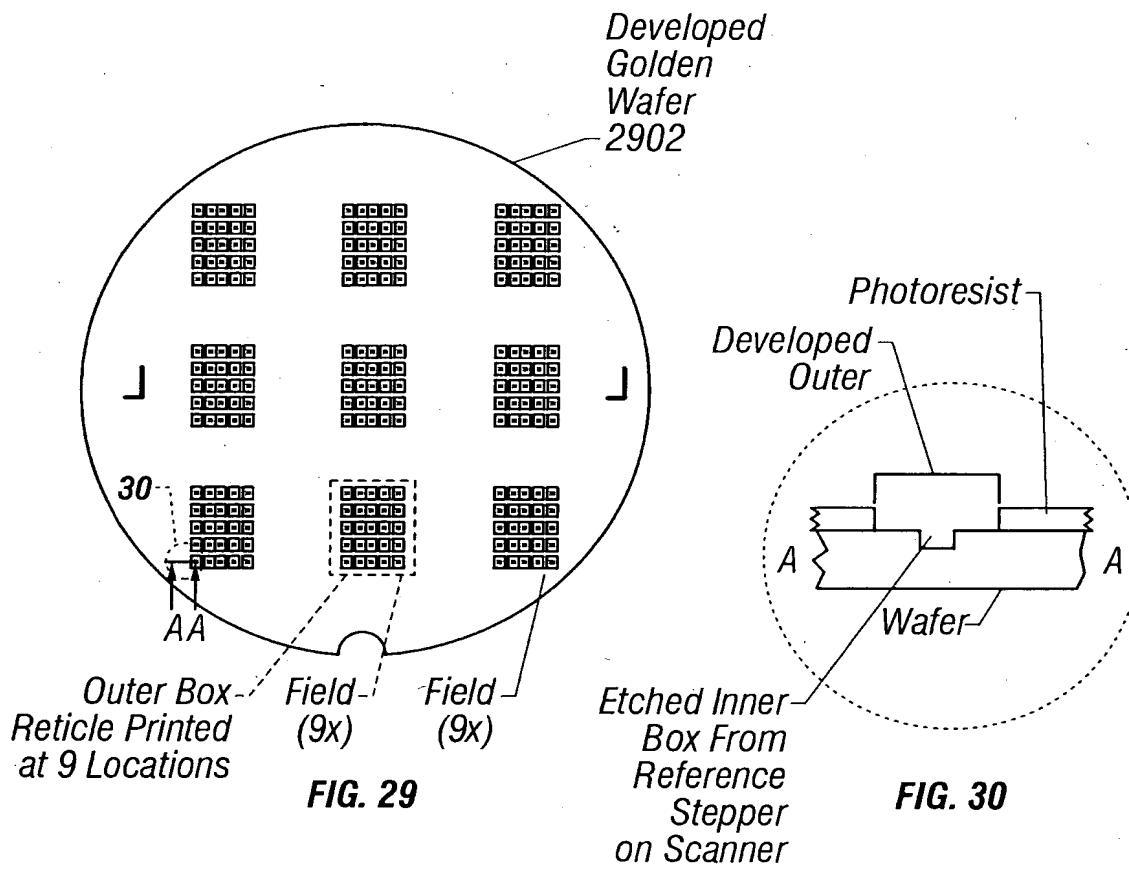
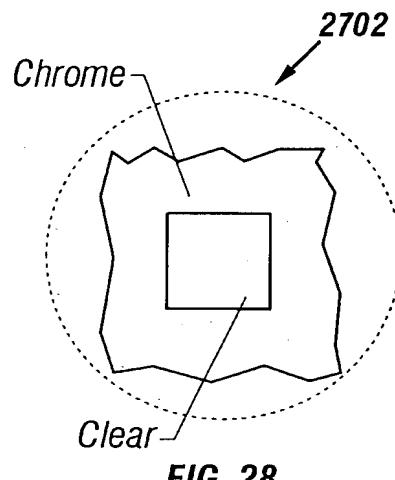
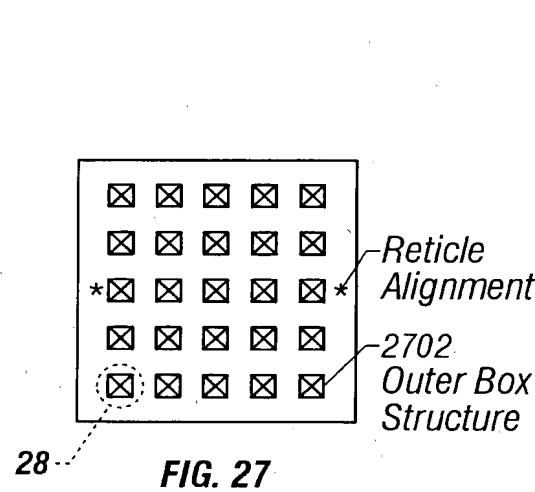


FIG. 25

FIG. 26



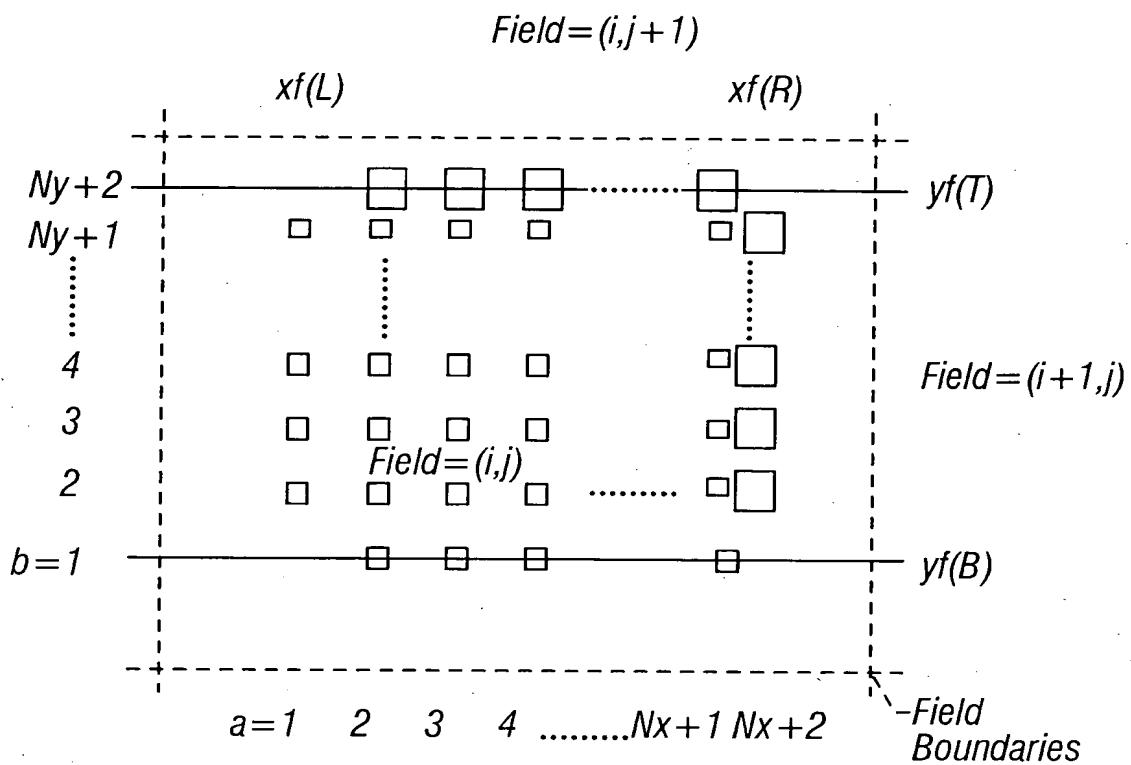


FIG. 31

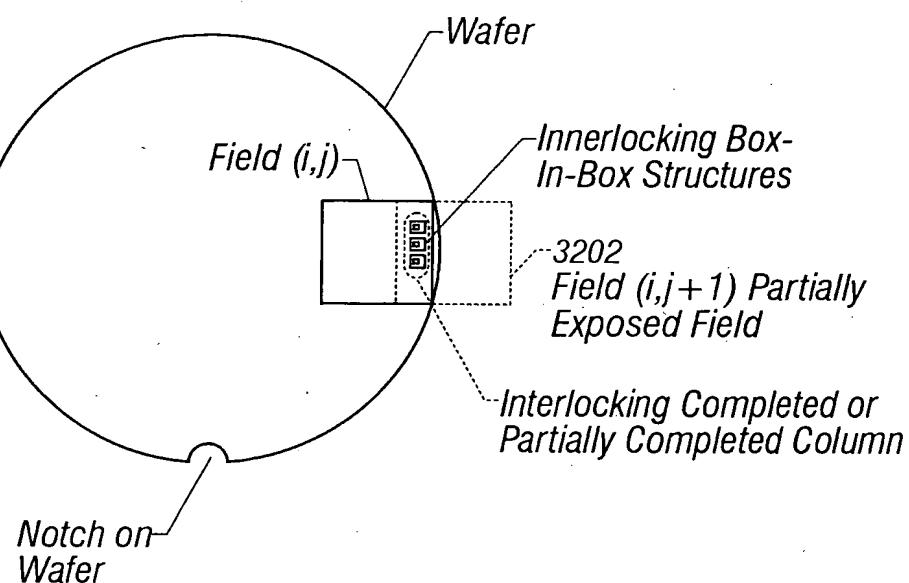


FIG. 32

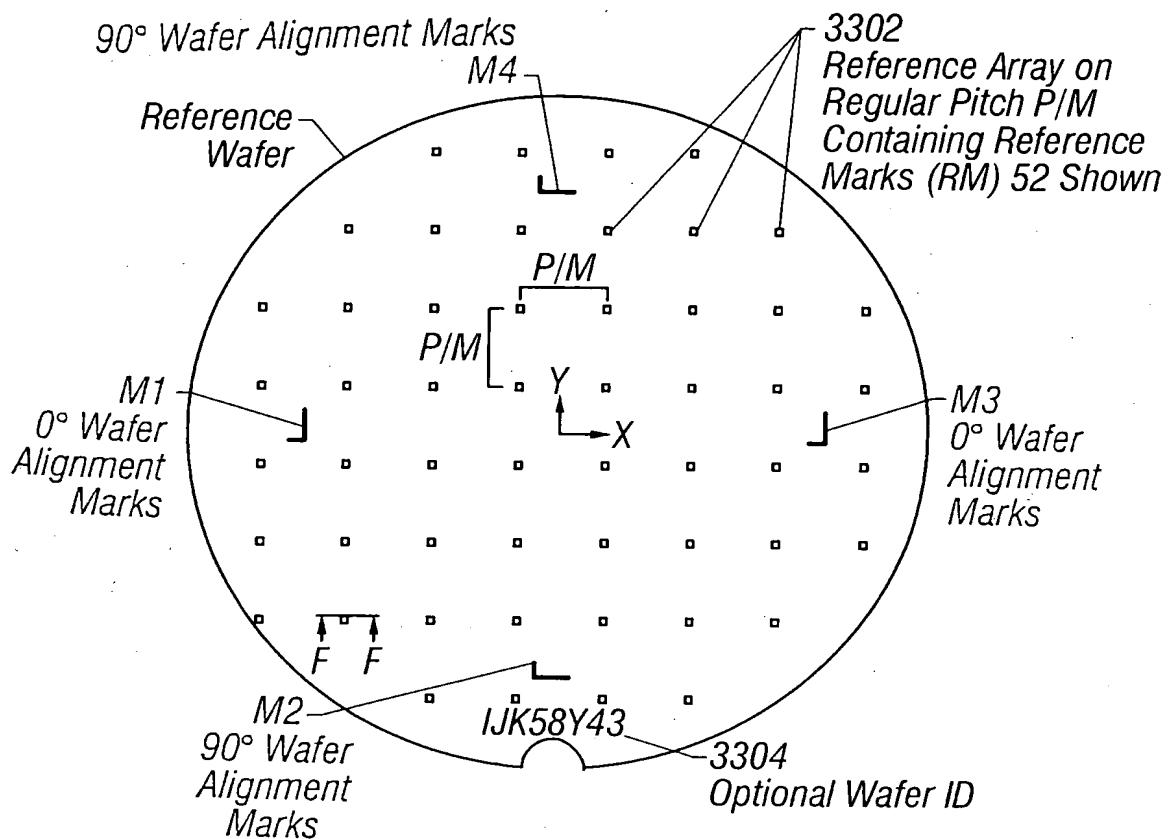
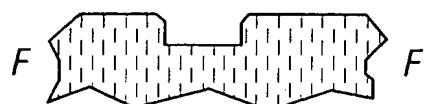


FIG. 33

Feature	xG	yG	dx	dy
M1	-95.000000	0.000000	0.000050	-0.000037
M2	0.000000	-95.000000	-0.000387	0.000298
M3	95.000000	0.000000	0.000499	-0.000799
M4	0.000000	95.000000	0.000174	0.000274
RM	10.000000	10.000000	0.000598	0.000420
RM	10.000000	20.000000	0.000495	-0.000229
⋮	⋮	⋮	⋮	⋮
RM	-60.000000	-80.000000	0.000339	0.000449

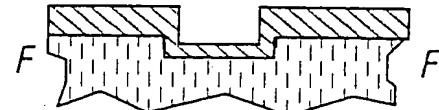
52
 Entries For Wafer
 of Figure 33

FIG. 34



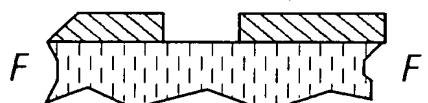
Pits in Wafer

FIG. 35A



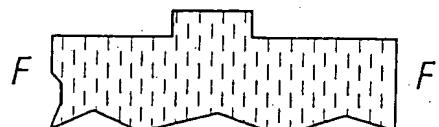
Pits in Wafer Overcoated

FIG. 35D



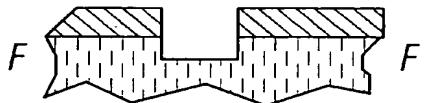
Pits in Overcoating

FIG. 35B



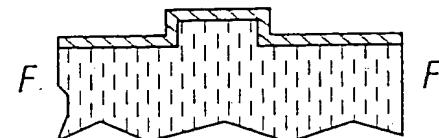
Mound in Wafer

FIG. 35E



Pits in Overcoating & Wafer

FIG. 35C



Overcoated Mound on Wafer

FIG. 35F

[Hatched Box] = Si or Substrate

[Diagonal Hatched Box] = Deposited of Overcoat Layer

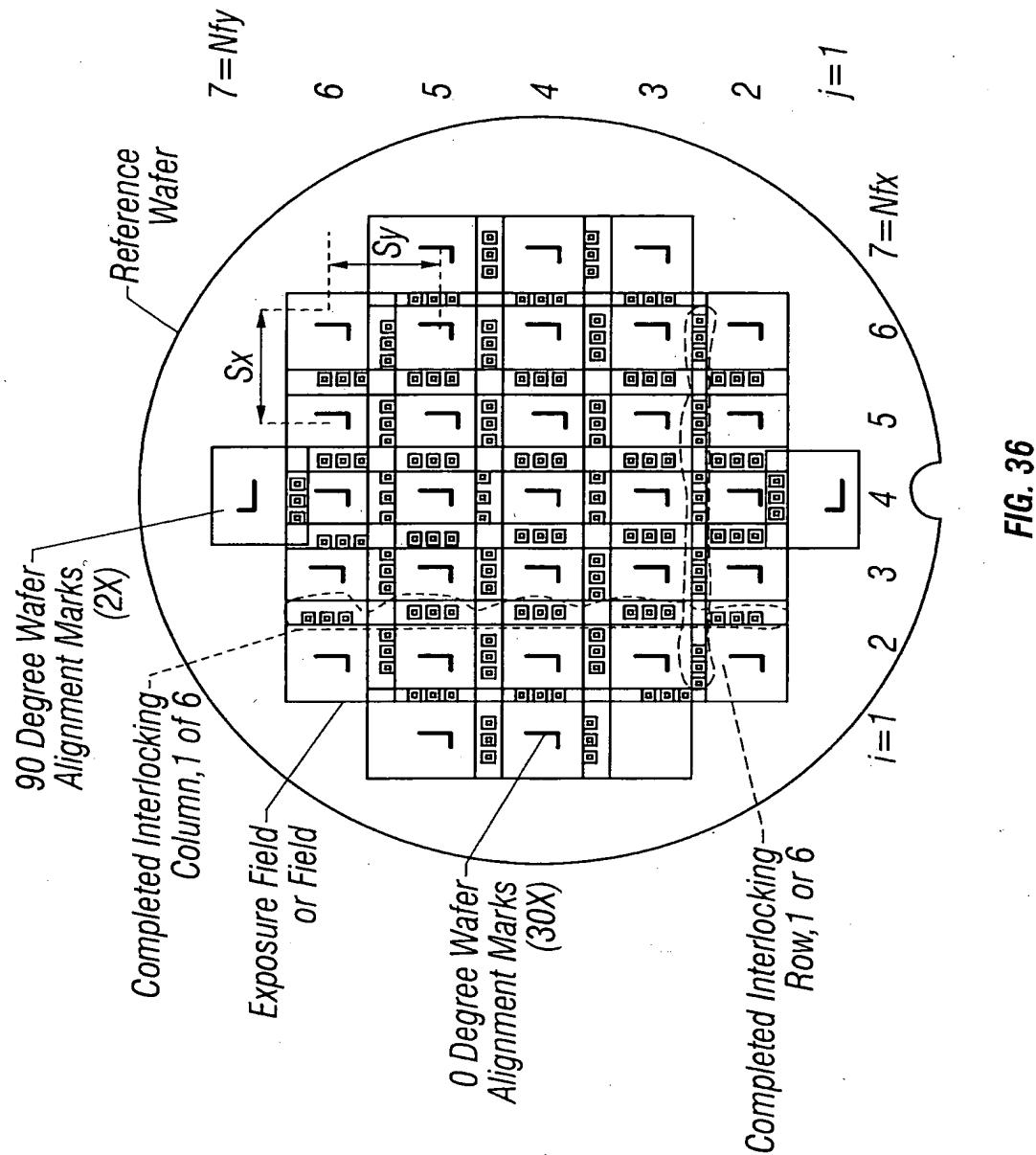


FIG. 36